WHAT IS CLAIMED IS:

1. A light emitting device with a pixel comprising:

a light emitting element;

a first transistor for determining a current value flowing in the light emitting element;

a second transistor for determining a light emission or non-emission of the light emitting element according to a video signal; and

a third transistor for determining an input of the video signal,

wherein the light emitting element is connected in series to the first transistor and the second transistor between a first power supply and a third power supply,

wherein a gate electrode of the third transistor is connected to a first scan line,

wherein a gate electrode of the first transistor is connected to a second scan line, and

wherein the first transistor is operated in a saturation region and the second transistor is operated in a linear region.

2. The light emitting device according to claim 1, wherein each of the first transistor and the second transistor has the

same conductivity.

3. The light emitting device according to claim 1, wherein the first transistor is a depletion mode transistor.

4. The light emitting device according to claim 1, wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width.

5. The light emitting device according to claim 4, a ratio of the channel length to the channel width of the first transistor is five or more.

6. An element substrate comprising a pixel comprising:

a pixel electrode;

a first transistor for determining a current value flowing in the light emitting element;

a second transistor for determining a light emission or non-emission of the light emitting element according to a video signal; and

a third transistor for controlling an input of the video signal,

wherein the first transistor is connected in series to the second transistor between a first power supply and a third power supply,

a gate electrode of the third transistor is connected to a first scan line,

a gate electrode of the first transistor is connected to a second scan line, and

wherein the first transistor is operated in a saturation region and the second transistor is operated in a linear region.

7. The element substrate according to claim 6, wherein each of the first transistor and the second transistor has the same conductivity.

8. The element substrate according to claim 6, wherein the first transistor is a depletion mode transistor.

9. The element substrate according to claim 6, wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width.

10. The element substrate according to claim 9, a ratio

of the channel length to the channel width of the first transistor is five or more.